

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	4	L1 and ((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (random near2 number near2 generator) "linear feedback shift register") same (deterministic near3 (data vector value bit)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/13 15:29
S63	4	S62 and ((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (random near2 number near2 generator) "linear feedback shift register") same (deterministic near3 (data vector value bit)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/13 15:28
S62	6571	(714/724,727,728,733-739,742).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/13 15:28
L1	7574	(714/724,727,728,733-739,742).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/13 15:28
S61	4	S60 and ((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (random near2 number near2 generator) "linear feedback shift register") same (deterministic near3 (data vector value bit)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 09:12
S60	6287	(714/724,727,728,733-739,742).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 09:11
S1	4	((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (random near2 number near2 generator) "linear feedback shift register") same (deterministic near3 (data vector value bit))) and ATPG and ((integrated near2 circuit) ASIC IC DUT device circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/12 15:48
S59	4	"534,015".ap.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/12 15:46

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S58	122	S57 and select\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 15:09
S57	165	S52 not S54	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 15:08
S56	49	S54 not S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 15:07
S55	5	S54 and deterministic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 15:00
S54	54	S52 and mask\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 14:57
S53	48	S52 and mask	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 14:57
S52	219	decompress\$3 near3 vector	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 14:57
S51	3	S50 and reseed\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 14:41
S50	10	(US-20020093356-\$ or US-20040064771-\$ or US-20040128599-\$).did. or (US-5991909-\$ or US-6061818-\$ or US-5383143-\$ or US-5444716-\$ or US-5983380-\$ or US-5612963-\$ or US-5029166-\$).did.	US-PGPUB; USPAT	OR	ON	2005/01/11 14:40
S49	1	"4872125".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:58

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S48	1	"4872169".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:58
S47	1	"5029166".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:50
S46	1	"5132635".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:50
S45	1	"3719885".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:47
S44	1	"5043988".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:46
S43	1	"5297151".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:46
S42	1	"5394405".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:46
S41	1	"5414716".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:46
S40	1	"5323400".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:46
S39	1	"4503537".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:45
S38	1	"4688223".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:45
S37	1	"4801870".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:43
S36	1	"4974184".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:39
S35	1	"5043988".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:35
S34	1	"5297151".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:35
S33	1	"5323400".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:34
S32	1	"5369648".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:33
S31	1	"5394405".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:33
S30	1	"5412665".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:32
S29	1	"5414716".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:32
S28	1	"5479414".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:31
S27	1	"5485471".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:31

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S26	1	"5612963".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:31
S25	1	"5617531".PN.	USPAT; USOCR	OR	ON	2005/01/11 13:30
S24	4	("5983380" "5612963").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 13:08
S23	4	("5983380" "5612969").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 13:08
S22	24	S20 and ((LFSR (pseudo near2 random) "linear feedback shift register") (ATPG (automatic\$4 near2 test\$3)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 11:38
S21	21	S20 and (LFSR (pseudo near2 random) "linear feedback shift register")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 11:37
S15	5	((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (pseudo near2 random) "linear feedback shift register") same ((deterministic near3 (data vector value bit pattern)) near5 (\$3ROM memory)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 11:36
S20	639	S17 and (compress\$3 near3 (data vector code bit) same memory \$3ROM)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 11:35
S19	59	S17 and (compressed near3 data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 11:29
S18	61443	S17 compressed with data	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 11:22
S17	1410	((select\$3 multiplex\$3 switch\$3 mux\$3) same ((mask\$3 near3 (data vector value bit pattern)) near5 (\$3ROM memory)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 11:22

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S16	28	((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (pseudo near2 random) "linear feedback shift register") same ((\$3determin\$5 near3 (data vector value bit pattern)) near5 (\$3ROM memory)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/11 11:13
S13	35	((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (pseudo near2 random) "linear feedback shift register") same (deterministic near3 (data vector value bit pattern))) and ((integrated near2 circuit) ASIC IC DUT device circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 16:09
S14	7	S13 and ((seed seeding reseed reseeding) near4 (LFSR (pseudo near2 random) "linear feedback shift register")) and compress\$3 and decompress\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 15:15
S12	175	S11 and compress\$3 and decompress\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 15:15
S11	522	S8 and ((seed seeding reseed reseeding) near4 (LFSR (pseudo near2 random) "linear feedback shift register"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 15:15
S8	4505	((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (pseudo near2 random) "linear feedback shift register") same (data vector value bit pattern)) and ((integrated near2 circuit) ASIC IC DUT device circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 15:13
S10	24	S9 and compress\$3 and decompress\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 15:11
S9	46	S8 and (mask\$3 near3 (data vector bit pattern)) and ((seed seeding reseed reseeding) near4 (LFSR (pseudo near2 random) "linear feedback shift register"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 15:10
S5	10	S4 and compress\$3 and decompress\$3 and (mask\$3 near3 (data vector bit)) and seed	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 15:05

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S7	4229	((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (pseudo near2 random) "linear feedback shift register") same (data vector value bit)) and ((integrated near2 circuit) ASIC IC DUT device circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 15:04
S6	27	S4 and (mask\$3 near3 (data vector bit)) and ((seed seeding reseed reseeding) near4 (LFSR (pseudo near2 random near2 number) "linear feedback shift register"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 15:04
S4	1830	((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (pseudo near2 random near2 number) "linear feedback shift register") same (data vector value bit)) and ((integrated near2 circuit) ASIC IC DUT device circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 15:03
S3	14	((select\$3 multiplex\$3 switch\$3 mux\$3) same (LFSR (pseudo near2 random near2 number) "linear feedback shift register") same (deterministic near3 (data vector value bit))) and ((integrated near2 circuit) ASIC IC DUT device circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 14:53
S2	2	S1 and (tester ATE)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/10 14:09